CLAIMS

1. (currently amended) A method for ~~capturing simulation output~~ testing an integrated circuit, comprising:

providing a stimulus to a test bench;

providing a device model corresponding to ~~an~~ the integrated circuit to the test bench; and

in response to applying the stimulus to the device model through the test bench,

generating a captured simulation, the captured simulation comprising information related to at least one of strobe timing information, opcode information, mixed signal information, and internal memory content information; and

testing the integrated circuit using the captured simulation.

2. (original) The method of claim 1, wherein the captured simulation comprises sufficient information for automatically generating a complete test pattern within a test program corresponding to the integrated circuit.

3. (original) The method of claim 1, wherein the captured simulation captures all communication through the test bench between the stimulus and the device model.

4. (original) The method of claim 1, wherein the stimulus and the test bench communicate in accordance with a predetermined protocol which provides a standard interface between the stimulus and the test bench.

5. (original) The method of claim 1, wherein the device model and the test bench communicate in accordance with a predetermined protocol which provides a standard interface between the device model and the test bench.

6. (original) The method of claim 5, wherein all communication with the device model occurs through the standard interface between the device model and the test bench.

7. (original) The method of claim 1, wherein the stimulus comprises verification patterns, drivers, and monitors.

8. (original) The method of claim 7, wherein the stimulus further comprises a simulation environment corresponding to the device model.

9. (original) The method of claim 1, wherein:

in response to applying the stimulus to the device model through the test bench, the test bench generates a plurality of simulation parameters corresponding to the stimulus and device model; and

the captured simulation is based at least in part on the simulation parameters.

10. (original) The method of claim 1, wherein the captured simulation comprises information relating to another one of strobe timing information, opcode information, mixed signal information, and internal memory content information.

11. (original) The method of claim 1, wherein the captured simulation further comprises information relating to at least one of directionality information, pin data information, masking information, comment information, and partial cyclized information.

12. (Currently Amended) A method for ~~preparing a captured simulation for post-processing~~ testing an integrated circuit, comprising:

~~receiving the~~ providing a captured simulation in response to applying a stimulus to a device model of the integrated circuit, wherein the captured simulation comprises at least one of strobe timing information, opcode information, mixed signal information, and internal memory content information, the captured simulation generated in response to stimulus applied to a device model through a test bench;

generating data patterns based at least in part on the one of strobe timing information, opcode information, mixed signal information, and internal memory content information, the data patterns capable of being retargettable for a plurality of post-processing tools; ~~and~~

providing a first formatted pattern file to a first post-processing tool, the first formatted pattern file based on the data patterns; and

using the first post-processing tool to test the integrated circuit.

13. (original) The method of claim 12, wherein the captured simulation comprises another one of strobe timing information, opcode information, mixed signal information, and internal memory content, and generating the data patterns is further based at least in part on the another one of strobe timing information, opcode information, and mixed signal information, and internal memory content information.

14. (original) The method of claim 12, wherein the captured simulation further comprises information relating to at least one of directionality information, pin data information, masking information, comment information, and partial cyclized information.

15. (original) The method of claim 12, wherein the data patterns include cyclized patterns.

16. (original) The method of claim 12, wherein the first post-processing tool is one of a fault simulator, virtual tester, and automatic test equipment (ATE) tester.

17. (original) The method of claim 16, further comprising:

providing a second formatted pattern file to a second post-processing tool, the second formatted pattern file based on the data patterns and wherein the second post-processing tool is another one of a fault simulator, virtual tester, and automatic test equipment (ATE) tester.

18. (currently amended) A testing system for testing an integrated circuit ~~data pattern generator stored via a computer readable medium~~, comprising:

simulation means for providing a captured simulation in response to applying a stimulus to a device model of the integrated circuit;

first instruction means for receiving the captured simulation wherein the captured simulation comprises at least one of strobe timing information, opcode information,

mixed signal information, and internal memory content information, the captured simulation generated in response to stimulus applied to a device model through a test bench;

second instruction means for generating data patterns based at least in part on the one of strobe timing information, opcode information, mixed signal information, and internal memory content information, the data patterns capable of being retargettable for a plurality of post-processing tools; and

third instruction means for providing a first formatted pattern file to a first post-processing tool, the first formatted pattern file based on the data patterns, wherein the first-processing tool is for testing the integrated circuit using the first formatted pattern file.

19. (currently amended) The ~~data pattern generator~~ testing system of claim 18, wherein the captured simulation comprises another one of strobe timing information, opcode information, and mixed signal information, and generating the data patterns is further based at least in part on the another one of strobe timing information, opcode information, and mixed signal information.

20. (currently amended) The ~~data pattern generator~~ testing system of claim 18, wherein the first post-processing tool is one of a fault simulator, virtual tester, and automatic test equipment (ATE) tester.

21. (currently amended) The ~~data pattern generator~~ testing system of claim 20, further comprising:

fourth instruction means for providing a second formatted pattern file to a second post-processing tool, the second formatted pattern file based on the data patterns and wherein the second post-processing tool is another one of a fault simulator, virtual tester, and automatic test equipment (ATE) tester.

22. (currently amended) A testing system for testing an integrated circuit ~~standard reusable test bench stored via a computer readable medium~~, comprising:

first instruction means for receiving a stimulus;

second instruction means for receiving a device model corresponding to an integrated circuit; and

third instruction means for generating simulation parameters in response to applying the stimulus to the device model;

fourth instruction means for creating a captured simulation based at least in part on the simulation parameters, the captured simulation comprising information related to at least one of strobe timing information, opcode information, mixed signal information, and internal memory content information; and

tester means for testing the integrated circuit using the captured simulation.

23. (currently amended) The ~~standard reusable test bench~~ testing system of claim 22, wherein the captured simulation comprises sufficient information for automatically generating a complete test within a test program corresponding to the integrated circuit.

24. (currently amended) The ~~standard reusable test bench~~ testing system of claim 22, wherein the captured simulation captures all communication between the stimulus and the device model through the standard reusable test bench.

25. (currently amended) The ~~standard reusable test bench~~ testing system of claim 22, wherein all communication with the device model occurs through the standard reusable test bench.

26. (currently amended) The ~~standard reusable test bench~~ testing system of claim 22, wherein the captured simulation comprises information relating to another one of strobe timing information, opcode information, mixed signal information, and internal memory content information.

27. (currently amended) The ~~standard reusable test bench~~ testing system of claim 22, wherein the captured simulation comprises information relating to at least one of directionality information, pin data information, masking information, comment information, and partial cyclized information.